CH7521A 4 Lane DisplayPort to 6 Channel LVDS Controller

FEATURES

General

- Compliant with DisplayPort specification version 1.2 and Embedded DisplayPort (eDP) specification version 1.2
- Support VESA and CEA timing standards up to 7680x1080@60Hz or 4096x2160@60Hz with 8/10 bit graphic color depth
- Support Single Port, Dual Ports , Quad ports and Six ports LVDS output interface
- Crystal Free
- Built in self test mode support
- Hot Plug Detection
- Dither support from 10 bit to 8 bit and 8 bit to 6 bit
- Region CRC checking support
- Black panel or Color Bar during invalid input and failure detection
- 16-pixel overlay on the Left and Right sides support, and enabled by the internal register
- Initiated and controlled by firmware which is loaded from External BOOT ROM automatically upon power up
- integrated EDID Buffer up to 2 blocks
- Firmware updated through I2C slave or AUX Channel
- I2C slave support up to 400K Hz
- Programmable power management
- Achieve bit error rate $<10^{-9}$ for raw transport data per lane and symbol error rate <10-12 for control data
- Low power consumption
- ESD HBM 4KV
- Offered in a 128-pin QFN package (12.5 x 12.5mm)

DP Receiver

- Compliant with DisplayPort Specification version 1.2 and Embedded DisplayPort (eDP) Specification version 1.2
- Support 4 Main Link Lanes at 1.62Gb/s, 2.7Gb/s or 5.4Gb/s link rate
- Supports input color depth 6, 8 or 10-bit per pixel in RGB format
- Supports Flexible Lane swap and P/N signal polarity swap on the Main Link Lanes and the AUX channel
- Supports Enhanced Framing Mode
- Support dynamic refresh rate or adaptive sync mode
- Fast and full Link Training for DisplayPort system
- Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
- Support typical 0.5% down spread spectrum clock(SSC) DP input

LVDS Transmitter

- Support Single Port, Dual Ports , Quad ports and Six

GENERAL DESCRIPTION

Chrontel's CH7521A is a low-cost, low-power semiconductor device that translates the DisplayPort signal to the LVDS in form of RGB. This innovative DisplayPort receiver with integrated 6 channel LVDS transmitters is specially designed to target the Automotive market segments. Leveraging the DisplayPort's unique source/sink "Link Training" routine, the CH7521A is capable of instantly bring up the video display to the LCD when the initialization process is completed between CH7521A and the graphic chip.

The CH7521A is designed to meet the DisplayPort specification version 1.2 and the Embedded DisplayPort Specification version 1.2. The 4 Main Link Lanes receiver supports input with data rate running at 1.62Gb/s, 2.7Gb/s or 5.4Gb/s, and can accept digital RGB signal for LVDS output up to 7680x1080@60Hz or 4096x2160@60Hz .

The CH7521A will convert the DisplayPort signal to LVDS output after DisplayPort Link Training is completed. This feature can be achieved by loading the panel's EDID and the CH7521A's configuration settings in the serial external BOOT ROM connected to the CH7521A. During system power-up and upon completion of the DisplayPort Link Training through AUX Channel, CH7521A will generate LVDS signal according to the panel power-up timing sequencing stored in the external BOOT ROM.

Advanced Region CRC checking and signal failure detection module and the related interrupt mechanism is incorporated in CH7521A, which is specially designed to reduce the risk of signal transmission error in normal consumer or industrial operation.

ports LVDS output interface with 6/8/10 bit color depth
- Single LVDS port supports up to 140MHz pixel clock frequency
- Support 3 sets TDDI/DDIC Connection with dual LVDS ports for each set, and 4 sets TDDI/DDIC Connection with single LVDS port for each set
- Support both OpenLDI (or JEIDA), SPWG (or VESA) and non-JEITA (10-bit only) bit mapping for LVDS application
- LVDS Tx FFE support up to 3 dB Gain
- Flexible LVDS Port Assignment support
- Flexible LVDS output pins swapping
- Spread spectrum control is available for transmitting LVDS signal
- Signal slew rate control is available for the transmitting LVDS signal
- Programmable LVDS Swing and Common Voltage

APPLICATION

- AIO
- Pro-AV system
- Terminal Display Device

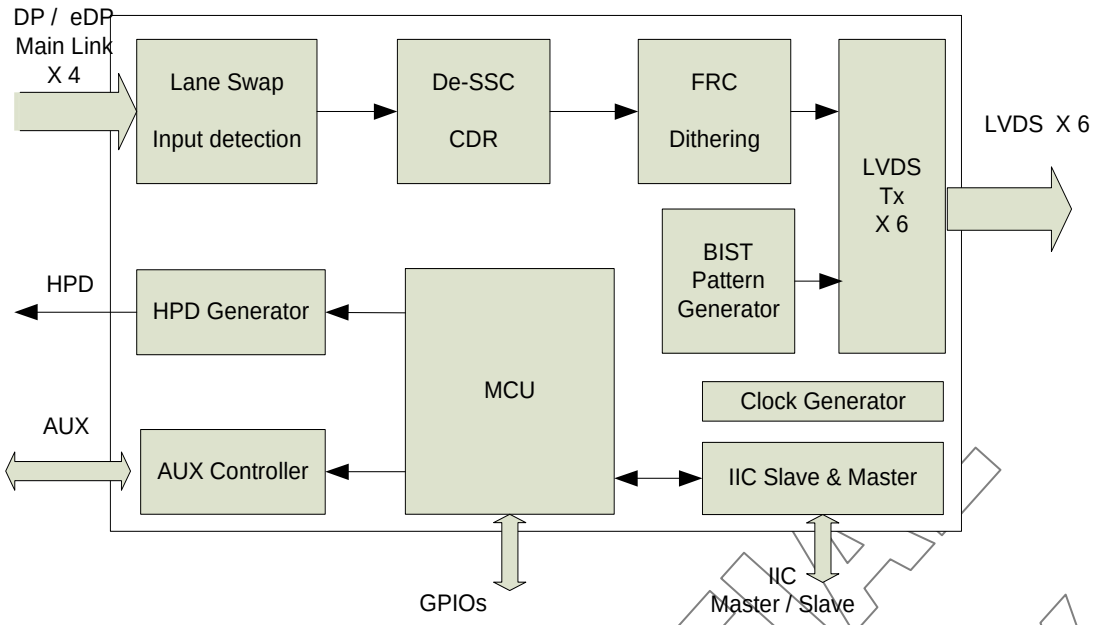

Figure 1: CH7521A Functional Block Diagram

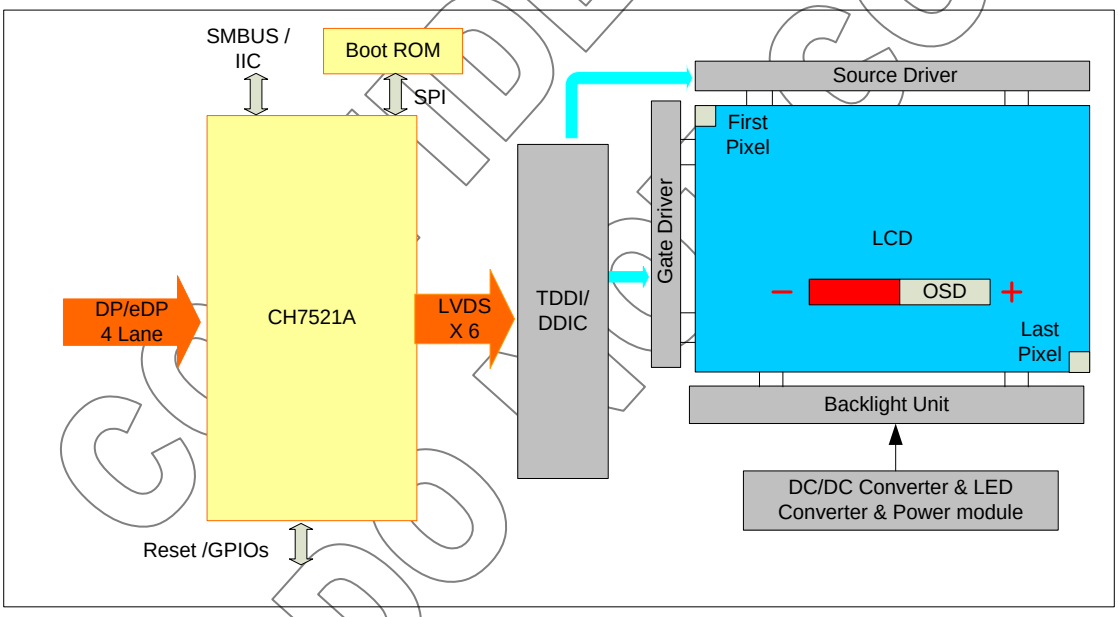

Figure 2: CH7521A Application Diagram

1.0 PIN-OUT

1.1 Package Diagram

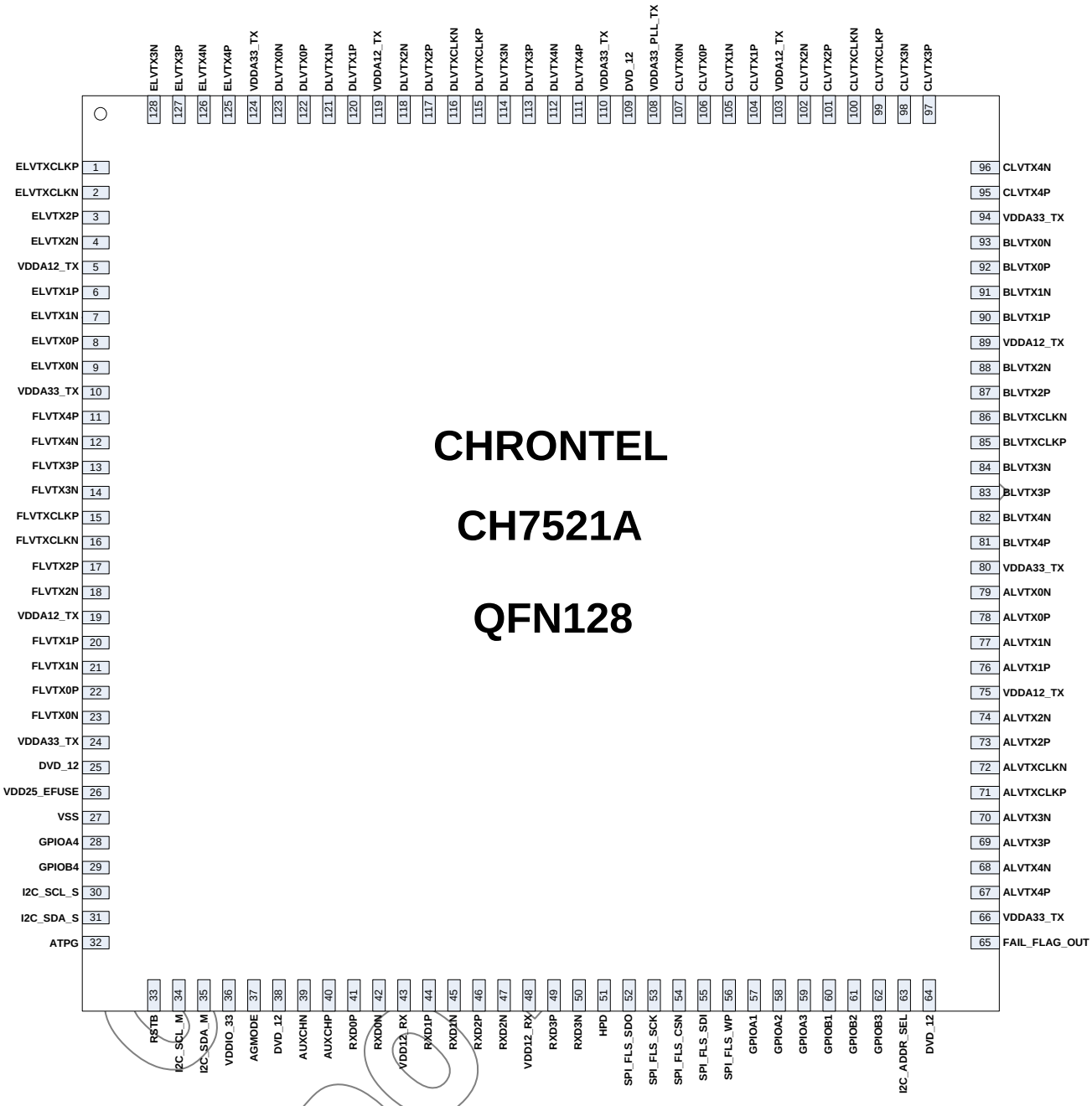

Figure 3: CH7521A 128-Pin QFN Pin Out

1.2 Pin Description

Table 1: CH7521A Pin Description

Pin #	Type	Symbol	Description
1~4,6~9,125~128	Out	ELVTX[4:0], ELVTXCLKP/N	**The Fifth Channel LVDS Output**
11~18,20~23	Out	FLVTX[4:0], FLVTXCLKP/N	**The Sixth Channel LVDS Output**
67~74,76~79	Out	ALVTX[4:0] P/N, ALVTXCLKP/N	**The First Channel LVDS Output**
81~88,90~93	Out	BLVTX[4:0], BLVTXCLKP/N	**The Second Channel LVDS Output**
95~102,104~107	Out	CLVTX[4:0], CLVTXCLKP/N	**The Third Channel LVDS Output**
111~118,120~123	Out	DLVTX[4:0], DLVTXCLKP/N	**The Fourth Channel LVDS Output**
28,57~59	In/Out	GPIOA[4:1]	**General Purpose Input/Output**
29,60~62	In/Out	GPIOB[4:1]	**General Purpose Input/Output**
30	In	I2C_SCL_S	**Serial Port Clock Input for CH7521A IIC Slave** This pin functions as the clock input of the serial port and operates with inputs from 0 to 3.3V. This pin requires an external 4kΩ - 9kΩ pull up resistor to 3.3V.
31	In/Out	I2C_SDA_S	**Serial Port Data Input / Output for CH7521A IIC Slave** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 3.3V. Outputs are driven from 0 to 3.3V. This pin requires an external 4kΩ - 9 kΩ pull up resistor to 3.3V.
32		ATPG	**Test Pin**
33	In	RSTB	**Reset* Input (Internal pull-up)** When this pin is pull low, the device is held in the power-on reset condition. When this pin is pull high, reset is controlled through the serial port register.
34	Out	I2C_SCL_M	**Serial Port Clock Output for EDID/HDCP ROM** This pin functions as the clock output of the serial port and operates with output from 0 to 3.3V. This pin requires an external 4kΩ - 9kΩ pull up resistor to 3.3V.
35	In/Out	I2C_SDA_M	**Serial Port Data Input/Output for EDID/HDCP ROM** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 3.3V. Outputs are driven from 0 to 3.3V. This pin requires an external 4kΩ - 9 kΩ pull up resistor to 3.3V.
37	In	AGMODE	**Aging Pattern Selection** AGMODE=H: and no video in: BIST pattern AGMODE=L: and no video in: black pattern (default)
39,40	In/Out	AUXCHP/N	**Aux Channel Differential Input/Output** These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal**.**
41,42,44~47, 49,50	In	RXD[3:0]P/N	**DisplayPort Lane 0~3 Input** One pair of differential data input. It handles clock-embedded high speed differential data input as DisplayPort standard
51	Out	HPD	**Hot Plug Detect** This output pin indicates whether this device is active or not. It also generates interrupt pulse as defined by DisplayPort standard. Output voltage is 3.3v.
52~56	In/Out	SPI_FLS_WP SPI_FLS _SDI SPI_FLS _CSN	**SPI interface for Boot ROM**

		SPI_FLS _SCK SPI_FLS _SDO	
63	In	I2C_ADDR_SEL	**IIC Slave Address Selection**
65	Out	FAIL_FLAG_OUT	**Fail Flag Output**
36	Power	VDDIO_33	**Digital I/O Power Supply (3.3V)**
25,38,64,109	Power	DVD_12	**Digital Power Supply (1.25V)**
43,48	Power	VDD12_RX	**DP Rx Power Supply (1.25V)**
10,24,66,80,94,110,124	Power	VDDA33_TX	**LVDS Power Supply (3.3V)**
5,19,75,89,103,119	Power	VDDA12_TX	**LVDS Analog Power Supply (1.25V)**
108	Power	VDDA33_PLL_TX	**LVDS PLL Power Supply (3.3V)**
26	Power	VDD25_EFUSE	**Internal Trimming Module Power Supply(2.5V)**
26, E-PAD	Power	VSS	**Ground**

2.0 PACKAGE DIMENSIONS

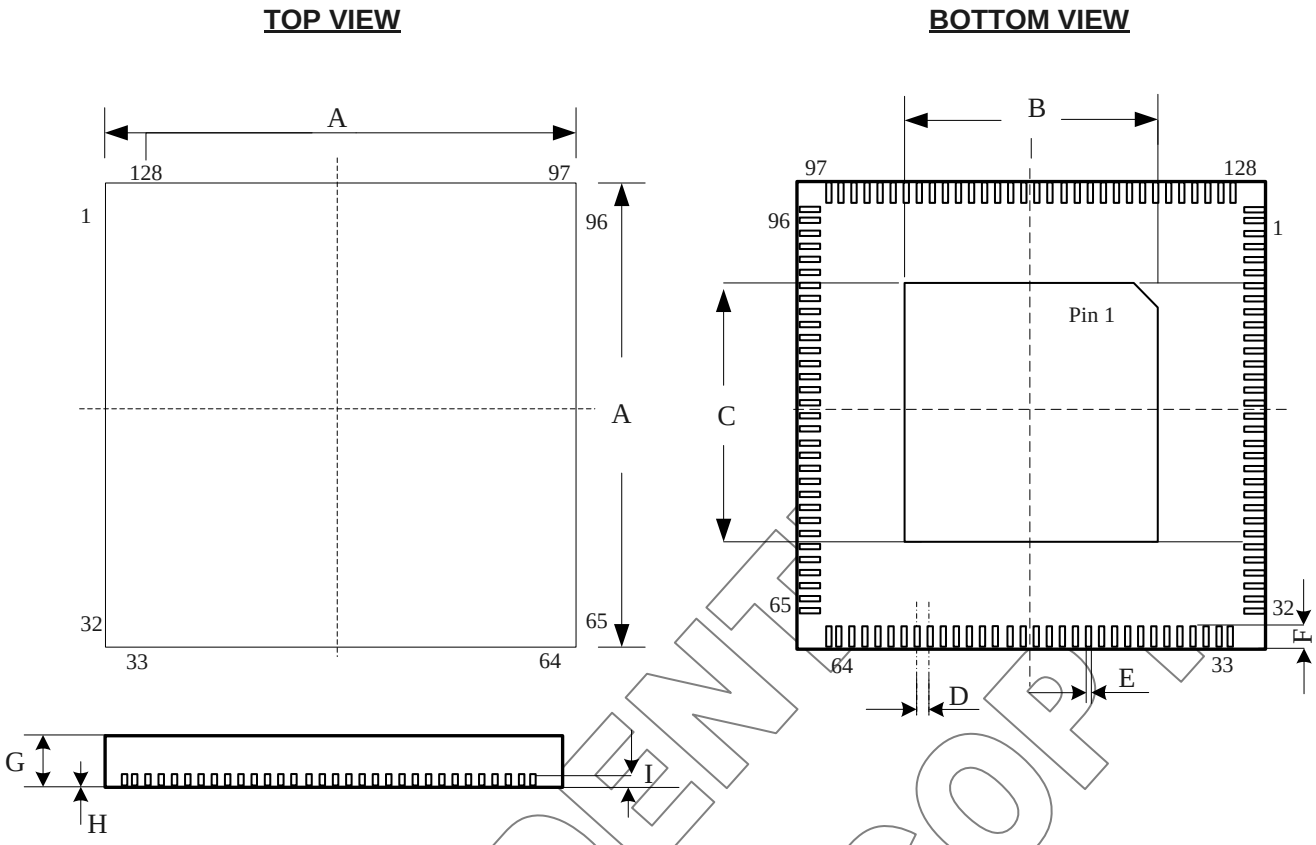

Figure 4: 128 QFN Package (12.5x12.5 mm)

Table of Dimensions

No. of Leads		SYMBOL								
128 (12.5x12.5 mm)		A	B	C	D	E	F	G	H	I
Milli- meters	MIN	12.4	6.5	6.5	0.35	0.1	0.3	0.7	0	0.15REF
	MAX	12.6	6.7	6.7	BSC	0.2	0.5	0.8	0.05	

Notes:

1. All dimensions conform to JEDEC standard MO-207.

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ORDERING INFORMATION			
Part Number	**Package Type**	**Operating Temperature Range**	**Minimum Order Quantity**
CH7521A-BF	128 QFN, Lead-free	Commercial: 0 to 70°C	90/Tray
CH7521A-BFI	128 QFN, Lead-free	Industrial: -40 to 85°C	90/Tray

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